REMARKS

Claims 1-12, 14, 16 and 18-19 were presented for examination. Claims 1-12, 14, 16 and 18-19 were rejected. The pending claims have been included herein for the Examiner's convenience. Reconsideration of this application and allowance of all pending claims are hereby respectfully requested.

The Applicant would like to thank the Examiner for the interview conducted on June 14, 2004. In the interview, the Applicant's representative explained the previously submitted arguments with respect to independent claims 1, 12 and 16 and Emma (U.S. Patent No. 5,619,665). More specifically, in Emma, there is selection between a conventional instruction and corresponding translated instruction. In the claimed invention, however, the selector makes a selection between a translated instruction from the output of the translator and a translated instruction that resides in the instruction cache. The Examiner acknowledged that he misunderstood the previously submitted arguments and agreed to reconsider the pending claims.

Rejection under 35 U.S.C. § 102

Claims 1 and 12, 14, 16 and 18 were rejected under 35 U.S.C. § 102 as being anticipated by Emma (U.S. Patent No. 5,619,665). This rejection is respectfully traversed. Applicant respectfully requests reconsideration and allowance of the claims in view of the following arguments. For at least the reasons stated below, Emma does not disclose or suggest each and every element of the claimed invention.

The present invention, as recited in independent claim 1 for example, relates to an instruction translator for a processor. The translator receives a non-native architecture instruction and translates the non-native architecture instruction into one or more corresponding

instruction(s). A selector provides an instruction to the processor for execution. The selector determines whether to provide a translated instruction from the instruction cache or a translated instruction from the translator.

Emma does not disclose or suggest "a selector ... for selectively outputting ... an instruction output by said translator and the corresponding instruction held in said instruction cache" as recited in independent claim 1. In contrast to the Applicant's claimed invention, Emma describes an arrangement for extending an instruction set architecture to encompass new instructions. In Emma, when a sequence of conventional instructions can be translated into extended architecture instructions, the resulting translated instructions are stored in the extended instruction (EI) cache (*See* Emma at FIG. 5 and col. 12, lines 17-23). The instruction (I) cache stores the conventional instructions. During a fetch operation, the EI cache is first accessed to determine if a corresponding translated instruction exists. If a translated instruction exists, then it is provided to the processor for execution. If a translated instruction does not exist, the conventional instruction is provided from the I cache to the processor for execution (*See* Emma at col. 12, lines 3-13).

More specifically, the execution of a translated, extended architecture instruction occurs *only if* it is possible to translate the conventional instruction (*See* Emma at col. 10, lines 4-10). In Emma, the processor may execute a conventional instruction or a translated instruction depending on whether the conventional instruction can be translated.

One advantage of the claimed invention is that the processor receives instructions in the first instruction architecture and need not be capable of executing instructions in multiple instruction set architectures. Thus Emma does not disclose or suggest the claimed features of selecting an instruction in the first architecture from the translator or the instruction cache.

Regarding independent claims 12 and 16, Emma similarly does not disclose or suggest each of the required claim elements. Claim 12 has been amended to recite "a selector ... for selectively outputting ... an instruction output by said translator and the corresponding instruction held in said instruction cache." For at least the reasons stated above with respect to claim 1, Emma does not disclose or suggest a selector having the claimed function.

Additionally, claim 16 has been amended to include "a second instruction storage unit" and "an instruction reading circuit ... for applying an instruction in said first instruction architecture output from said second instruction storage unit to said processor." The first instruction memory stores instructed that have been translated into a first architecture and the second instruction memory also stores instructions in the first architecture. As described above, Emma fails to disclose or suggest providing the processor with instructions having a single instruction architecture.

Dependent claims 2-11, 14 and 18 were also rejected as being anticipated by Emma. These claims depend from the independent claims and include additional patentable recitations. Accordingly, these claims should also be considered allowable over Emma for at least the reasons specified above. Reconsideration and withdrawal of the rejection are therefore respectfully requested.

Rejection under 35 U.S.C. § 103

Claims 2-11 and 19 have been rejected under 35 U.S.C. § 103 as being unpatentable over Emma in view of Dickol et al. (U.S. Patent No. 5,875,336, Goettelmann et al. (U.S. Patent No. 5,313,614), Gregor (U.S. Patent No. 5,023,776), and Schacham et al. (UK Patent Application GB220481A) in various combinations. Claims 2-11 and 19 depend from independent base

claims 1 and 16. Even if the proposed combination of references were proper, the proposed combination does not disclose or suggest each of the claim elements.

As described above, Emma fails to disclose or suggest at least the claimed feature of "a selector ... for selectively outputting ... an instruction output by said translator and the corresponding instruction held in said instruction cache" as recited in claim 1. Also, Emma fails to disclose or suggest "a second instruction storage unit" and "an instruction reading circuit ... for applying an instruction in said first instruction architecture output from said second instruction storage unit to said processor" as recited in amended claim 16. Even if proper, the proposed combination does not disclose the claimed invention, as Emma is deficient for at least the reasons described above. Applicant respectfully requests reconsideration and allowance of these claims.

Conclusion

Accordingly, it is believed that all pending claims are now in condition for allowance. Applicant therefore respectfully requests an early and favorable reconsideration and allowance of this application. If there are any outstanding issues which might be resolved by an interview or an Examiner's amendment, the Examiner is invited to call Applicant's representative at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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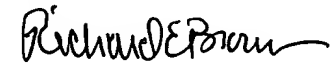

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